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EXAMINER	
JEANGLAUDE, JEAN BRUNER	
ART UNIT	**PAPER NUMBER**
2819	

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Please find below and/or attached an Office communication concerning this application or proceeding.

AK

Office Action Summary	Application No.	Applicant(s)	
	10/719,508	LIN ET AL.	
	Examiner	Art Unit	
	Jean B. Jeanglaude	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *amendment filed on 09-09-05*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *33-55* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *33-55* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Response To Amendments/Arguments

1. Applicant's arguments filed on September 9, 2005 have been fully considered but they are not persuasive. Regarding the Applicant's argument on page 6, fourth and fifth paragraphs that "First, it is well known that prior art must contain a teaching or suggestion to make the proposed modification, In this regard, there is no teaching or suggestion in either Callahan or APA to make the proposed modification", the Examiner recognizes that references cannot be arbitrarily combined and that there must be some reason why one skilled in the art would be motivated to make the proposed combination of primary and secondary references. In re Nomiya, 184 USPQ 607 (CCPA 1975). However, there is no requirement that a motivation to make the modification be expressly articulated. The test for combining references is what the combination of disclosures taken as a whole would suggest to one of ordinary skill in the art. In re McLaughlin, 170 USPQ 209 (CCPA 1971). References are evaluated by what they suggest to one versed in the art. Rather than by their specific disclosures. In re Bozek, 163 USPQ 545 (CCPA) 1969.

2. Regarding the applicant's argument on page 7, first and 3rd paragraphs that "this can be accomplished by impermissible hindsight reconstruction", it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the invention was made, and does not include knowledge gleaned only from the applicant's disclosure, such a

reconstruction is proper. In re McLaughlin, 443 F. 2d 1392; 170 USPQ 209 (CCPA 1971).

3. Regarding the Applicant's on page 7, 5th paragraph that "inverter 124 cannot correspond to the claimed level-shifter", the Examiner maintains that Callahan, Jr. et al. discloses a level-shifter that would combine with the applicant's admitted prior art that would perform the same as the claimed invention (see col. 2, lines 1 – 13 in Callahan). It is the combination of Callahan, Jr et al. and the APA that renders the claim obvious.

For at least the above reasons the rejection is maintained as follows:

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 33 - 55 are rejected under 35 U.S.C. 103(a) as being unpatentable over Callahan, Jr. et al. (US patent Number 5,574,475) in view of the Applicant's admitted prior art (APA).

6. Regarding claim 33, Callahan, Jr. et al. discloses a driver circuit (fig. 7) for a display, comprising k voltage levels, where k is at least $2^{(n-1)}$ (note in fig. 7 that there is a VDD voltage that provides common voltage lines to transistors 110); an input receiving a digital input data having n bits for selecting one of the k voltage levels for driving the circuit (the data line including the input digital data a, b, c, d, e, f; 120, fig. 7);

an output having a first side (the negation of these data input lines that receives the data; 122, fig. 7); a plurality of digital signal lines coupled to the digital input data (142, fig. 7). Callahan et al. disclose a driver circuit for a display in which the number of the plurality of digital signal lines on the first side of the output is less than 2n, with the digital signal lines comprising a first set of digital signal lines associated with a first set of digital bits and a second set of digital signal lines associated with a second set of digital bits, the second set of digital bits being inverted from the first set of digital bits; and wherein n is a positive integer greater than 1 [in Callahan, Jr. et al. the number of plurality of digital signal lines on the first side of the output is an even number that corresponds to a six bit data input which is equal to the number of inputs the decoder has chosen for decoding purpose resulting to 64 possible outputs. In selecting n be grater than 1, i.e. n=2, 3, 4, 5, 6, the number of possible outputs is 4, 6, 8, 10,..., infinity. In substituting n by its corresponding value one obtains an even number. Also, it is noted that the output at the other side of the circuitry shown in fig. 7 is inverted.]. Callahan, Jr. et al. does not explicitly disclose a driver circuit that comprises a plurality of transistor groups each transistor group formed by a plurality of serially coupled transistors, each transistor group being coupled to a separate one of the voltage levels and the output from the first side of the output each transistor group having n controllable transistors, each controllable transistor having a gate controlled by one of the digital signal lines. However, the APA, in a related field, discloses a driver circuit for a display that comprises a plurality of transistor groups [M30, M31, M32, M33 (group 1); M20, M21, M22, M23 (group 2); M10, M11, M12, M13 (group 3); M00, M01, M02, M03

(group 4)]; each transistor group formed by a plurality of serially coupled transistors (each group of transistors mentioned are in series), each transistor group being coupled to a separate one of the voltage levels (group 1 is coupled to V3; Group 2 is coupled to V2; Group 3 is coupled to V2, Group 4 is coupled to V1) and the output from the first side of the output each transistor group having n controllable transistors, each controllable transistor having a gate controlled by one of the digital signal lines (fig. 3). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Callahan et al.'s system with that of the APA in order to provide a system that enables the use of polysilicon lines as both digital lines and controllable gates to improve the performance of the system.

7. Regarding claim 38, Callahan, Jr. et al. discloses a circuit (fig. 7), wherein each transistor group has a total of m transistors, with m being a positive integer that is greater than n (fig. 7)[as noted in fig. 7, there are a number of n and p-channel transistors].

8. Regarding claims 39, 45, Callahan, Jr. et al. discloses a driver circuit (fig. 7) for a display, comprising: k voltage levels, where k is at least $2^{(n-1)}$ (note in fig. 7 that there is a VDD voltage that provides common voltage lines to transistors 110); an input receiving a digital input data having n bits for selecting one of the k voltage levels for driving the circuit (the data line including the input digital data a, b, c, d, e, f; 120, fig. 7); an output having a first side (the negation of these data input lines that receives the data; 122, fig. 7); a plurality of digital signal lines coupled to the digital input data (142, fig. 7); a plurality of blocking transistors (112, 110) positioned between the input and

selected digital signal lines, with at least one of the digital signal lines being coupled to a gate of each of the blocking transistors for controlling each of the blocking transistors (fig. 7), and wherein n is a positive integer greater than 1 and m being a positive integer that is greater than 1 [when n is greater than 1, the output is an even number. In Callahan, Jr. et al. the number of plurality of digital signal lines on the first side of the output is an even number that corresponds to a six bit data input which is equal to the number of inputs the decoder has chosen for decoding purpose resulting to 64 possible outputs. In selecting n be grater than 1, i.e. n=2, 3, 4, 5, 6, the number of possible outputs is 4, 6, 8, 10,..., infinity. In substituting n by its corresponding value one obtains an even number]. Callahan, Jr. et al. does not explicitly disclose a driver circuit that comprises a plurality of transistor groups each transistor group formed by a plurality of serially coupled transistors, each transistor group being coupled to a separate one of the voltage levels and the output from the first side of the output each transistor group having n controllable transistors, each controllable transistor having a gate controlled by one of the digital signal lines. However, the APA, in a related field, discloses a driver circuit for a display that comprises a plurality of transistor groups [M30, M31, M32, M33 (group 1); M20, M21, M22, M23 (group 2); M10, M11, M12, M13 (group 3); M00, M01, M02, M03 (group 4)]; each transistor group formed by a plurality of serially coupled transistors (each group of transistors mentioned are in series), each transistor group being coupled to a separate one of the voltage levels (group 1 is coupled to V3; Group 2 is coupled to V2; Group 3 is coupled to V2, Group 4 is coupled to V1) and the output from the first side of the output each transistor group having n controllable transistors,

each controllable transistor having a gate controlled by one of the digital signal lines (fig. 3). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Callahan et al.'s system with that of the APA in order to provide a system that enables the use of polysilicon lines as both digital lines and controllable gates to improve the performance of the system.

9. Regarding claim 40, Callahan et al. does not specifically disclose that the circuit includes a buffer positioned between the input and each digital signal line, wherein the buffers for the digital signal lines that control the blocking transistors are larger in size than the other buffers. However, Callahan et al.;'s system does include a buffer (col. 2, lines 8 – 13) that fulfill the same function as claimed in the invention. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made that the combination of Callahan et al.'s system with that of the APA would achieve the same end result at the claimed invention.

10. Regarding claim 41, Callahan, Jr. et al. discloses a circuit (fig. 7), wherein each blocking transistor is either a NMOS switching gate (112) or a CMOS transfer gate (110).

11. Regarding claim 46, Callahan, Jr. et al. discloses a driver circuit (fig. 7) for a display, comprising: k voltage levels, where k is at least $2^{(n-1)}$ (note in fig. 7 that there is a VDD voltage that provides common voltage lines to transistors 110); an input receiving a digital input data having n bits for selecting one of the k voltage levels for driving the circuit (the data line including the input digital data a, b, c, d, e, f; 120, fig. 7); an output having a first side (the negation of these data input lines that receives the

data; 122, fig. 7); a plurality of digital signal lines coupled to the digital input data (142, fig. 7). Callahan, Jr. et al. does not explicitly disclose a driver circuit and a plurality of transistor groups each transistor group formed by a plurality of serially coupled transistors, each transistor group being coupled to a separate one of the voltage levels and the output from the first side of the output each transistor group having n controllable transistors, each controllable transistor having a gate controlled by one of the digital signal lines. However, the APA, in a related field, discloses a driver circuit for a display that comprises a plurality of transistor groups [M30, M31, M32, M33 (group 1); M20, M21, M22, M23 (group 2); M10, M11, M12, M13 (group 3); M00, M01, M02, M03 (group 4)]; each transistor group formed by a plurality of serially coupled transistors (each group of transistors mentioned are in series), each transistor group being coupled to a separate one of the voltage levels (group 1 is coupled to V3; Group 2 is coupled to V2; Group 3 is coupled to V2, Group 4 is coupled to V1) and the output from the first side of the output each transistor group having n controllable transistors, each controllable transistor having a gate controlled by one of the digital signal lines (fig. 3). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Callahan et al.'s system with that of the APA in order to provide a system that enables the use of polysilicon lines as both digital lines and controllable gates to improve the performance of the system.

12. Moreover, Callahan, Jr. et al. does not explicitly disclose a circuit wherein the number of the plurality of digital signal lines on the first side of the n bits for selecting one of the k output is equal to 2n-2, and wherein n is a positive integer that is greater

than 1. However, Callahan, Jr. et al. discloses the number of plurality of digital signal lines on the first side of the output is an even number that corresponds to a six bit data input which is equal to the number of inputs the decoder has chosen for decoding purpose resulting to 64 possible outputs. In selecting n be grater than 1, i.e. n=2, 3, 4, 5, 6, the number of possible outputs is 4, 6, 8, 10,..., infinity. In substituting n by its corresponding value one obtains an even number. Also, it is noted that the output at the other side of the circuitry shown in fig. 7 is inverted. Moreover, an artisan in the art would have chosen the number of inputs to be an odd number such as 5 bit inputs to achieve 32 possible outputs [for n = 2, 3, 4, 5, 6, the outputs will be 3, 5, 7, 9, 11]. Therefore, it would have been obvious to one of ordinary skill in the at the time the invention was made that Calhan, Jr. et al.'s system would perform the same function as the claimed invention in selecting the input as 5 bit inputs and one ordinary skill in the art would utilize the same procedure as disclosed in Callahan, Jr. et al. to achieve the same end result as the claimed invention.

13. Regarding claim 47, Callahan, Jr. et al. discloses a circuit (fig. 7) wherein the plurality of digital signal lines are polysilicon lines (col 12, lines 17 – 19).

14. Regarding claim 48, Callahan, Jr. et a. discloses a circuit (fig. 7) wherein a first of the digital signal lines is discontinued between two adjacent active regions to form a first digital segment carrying the digital signal, and a second digital segment carrying a digital signal that is inverted from the digital signal of the first digital segment (fig. 7)[as noted in fig. 7 of Callahan, Jr. et al. the input digital signals (a, b, c, d, e, f) enables the digital number present on the data lines to be decoded and then the cell selects a

switch so that the corresponding desired analog output is selected for output, thereby produces inverted signals at the output) (col 12, lines 35 – 39)].

15. Regarding claim 49, Callahan, Jr. et al. discloses a circuit (fig. 7) that comprises a plurality of blocking transistors (112, 110) positioned between the input and selected digital signal lines, with at least one of the digital signal lines being coupled to a gate of each of the blocking transistors for controlling each of the blocking transistors (fig. 7).

16. Regarding claim 50, Callahan, Jr. et al. discloses a circuit (fig. 7) further including a buffer positioned between the input and each digital signal line, wherein the buffers for the digital signal lines that control the blocking transistors are larger in size than the other buffers 9col 2, lines 5 – 10)[as noted in Callahan, Jr. et al. there is a level shifter that may shift voltage levels of data input buffers with the signal driver circuit, thereby there is a buffer (not label) that is located in the circuit].

17. Regarding claims 35 - 37, 42 - 44, Callahan, Jr. et al. discloses the limitations as discussed above but does explicitly disclose a circuit, wherein the signal lines on the first side of the output is equal to 2n-1 and a circuit wherein the number of the digital signal lines on the first side of the output is an odd number and a circuit in which the number of the plurality of digital signal lines on the first side of the output is equal to 2n-2. However, as noted in Callahan et al. the number of plurality of digital signal lines on the first side of the output is an even number that corresponds to a six bit data input which is equal to the number of inputs the decoder has chosen for decoding purpose resulting to 64 possible outputs. In selecting n be grater than 1, i.e. n=2, 3, 4, 5, 6, the number of possible outputs is 4, 6, 8, 10,..., infinity. In substituting n by its

corresponding value one obtains an even number. Also, it is noted that the output at the other side of the circuitry shown in fig. 7 is inverted. Moreover, an artisan in the art would have chosen the number of inputs to be an odd number such as 5 bit inputs to achieve 32 possible outputs [for n = 2, 3, 4, 5, 6, the outputs will be 3, 5, 7, 9, 11]. Therefore, it would have been obvious to one of ordinary skill in the at the time the invention was made that Calhan, Jr. et al.'s system would perform the same function as the claimed invention in selecting the input as 5 bit inputs and one ordinary skill in the art would utilize the same procedure as disclosed in Callahan, Jr. et al. to achieve the same end result as the claimed invention.

18. Regarding claim 51, Callahan, Jr. et al. discloses a driver circuit (fig. 7) for a display, comprising k voltage levels, where k is at least $2^{(n-1)}$ (note in fig. 7 that there is a VDD voltage that provides common voltage lines to the transistors 110); an input receiving a digital input data having n bits for selecting one of the k voltage levels for driving the circuit (the data line including the input digital data a, b, c, d, e, f; 120, fig. 7); an output having a first side (the negation of these data input lines that receives the data; 122, fig. 7). Callahan, Jr. et al. does not explicitly disclose a driver circuit and a plurality of transistor groups each transistor group formed by a plurality of serially coupled transistors, each transistor group being coupled to a separate one of the voltage levels and the output from the first side of the output each transistor group having n controllable transistors, each controllable transistor having a gate controlled by one of the digital signal lines. However, the APA, in a related field, discloses a driver circuit for a display that comprises a plurality of transistor groups [M30, M31, M32, M33

(group 1); M20, M21, M22, M23 (group 2); M10, M11, M12, M13 (group 3); M00, M01, M02, M03 (group 4)]; each transistor group formed by a plurality of serially coupled transistors (each group of transistors mentioned are in series), each transistor group being coupled to a separate one of the voltage levels (group 1 is coupled to V3; Group 2 is coupled to V2; Group 3 is coupled to V2, Group 4 is coupled to V1) and the output from the first side of the output each transistor group having n controllable transistors, each controllable transistor having a gate controlled by one of the digital signal lines (fig. 3). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Callahan et al.'s system with that of the APA in order to provide a system that enables the use of polysilicon lines as both digital lines and controllable gates to improve the performance of the system.

19. Moreover, regarding claim 51, Callahan, Jr. et al. does not explicitly disclose a driver circuit that comprises at least one level-shifter, each level-shifter associated with a digital signal line. However, it is noted in fig. 7 of Callahan, Jr. et al. an inverter 124 causes its input to shift in its voltage level which results in an inversion of the applied voltage (col 2, lines 1 – 13). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made that Callahan, Jr. et al.'s system would perform the same function as the claimed invention since the inverter described in Callahan, Jr. et al. would perform the function of shifting signal applied in the circuitry.

20. Regarding claim 52, Callahan, Jr. et al. discloses a circuit (fig. 7) wherein the plurality of digital signal lines are polysilicon lines (col 12, lines 17 – 19).

21. Regarding claim 53, Callahan, Jr. et a. discloses a circuit (fig. 7) wherein a first of the digital signal lines is discontinued between two adjacent active regions to form a first digital segment carrying the digital signal, and a second digital segment carrying a digital signal that is inverted from the digital signal of the first digital segment (fig. 7)[as noted in fig. 7 of Callahan, Jr. et al. the input digital signals (a, b, c, d, e, f) enables the digital number present on the data lines to be decoded and then the cell selects a switch so that the corresponding desired analog output is selected for output, thereby produces inverted signals at the output) (col 12, lines 35 – 39)].

22. Regarding claim 54, Callahan, Jr. et al. discloses a circuit (fig. 7) that comprises a plurality of blocking transistors (112, 110) positioned between the input and selected digital signal lines, with at least one of the digital signal lines being coupled to a gate of each of the blocking transistors for controlling each of the blocking transistors (fig. 7).

23. Regarding claim 55, Callahan, Jr. et al. discloses a circuit (fig. 7) wherein the digital signal line has at least two discontinued segments (126, 130), with a level shifter [inverter](124) coupling between the discontinued segments.

Conclusion

24. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jean B. Jeanglaude whose telephone number is 571-272-1804. The examiner can normally be reached on Monday - Friday 7:30 A. M. - 5:00 P.M..

The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jean Bruner Jeanglaude
Primary Examiner
November 15, 2005